# CH32F103 Datasheet

V1.32

## Overview

The CH32F1 is an industrial-grade general microcontroller based on 32-bit ARM®Cortex™-M3 core. The CH32F1 is equipped with clock security system, multi-level power management, general DMA controller and so on.

Especially, the CH32F1 provides 2 USB2.0 controllers. One of the controllers supports USB host/device integrated (low/full speed), multi-channel capacitive Touchkey detection (TKey) function and a 12-bit DAC module. The CH32F1 also provides abundant peripheral sources, such as multi-channel 12-bit ADC module, multiple timers, CAN communication controller, I2C/USART/SPI interface, etc., to meet various needs in the industrial, medical, consumer and other markets.

## Features

- **Core:**
  - 32-bit ARM Cortex-M3 core
  - Up to 72 MHz system clock frequency
  - Single-cycle multiplication and hardware division
  - Interrupt technology, Fault process mechanisl
- **Memory:**
  - 20 KB volatile data memory, SRAM
  - 64 KB user application program memory, CodeFlash
  - 3.75 KB system bootloader memory, BootLoader
  - 128 B system non-volatile configuration memory
  - 128 B custom information memory
- **Power management and low power:**
  - Supply range: 2.7V to 5.5V, GPIO synchronous supply voltage
  - Low-power modes: Sleep/Stop/Standby
  - $V_{BAT}$ supply for RTC and backup register independently
- **System clock, reset**
  - Built-in factory-trimmed 8 MHz RC oscillator
  - Built-in 40 KHz RC oscillator
  - Built-in PLL, optional CPU clock up to 72MHz
  - External 4 to 16 MHz high-speed oscillator
  - External 32.768 KHz low-speed oscillator
  - Power-on/power-down reset (POR/PDR), programmable voltage detector (PVD)
- **Real-time clock (RTC): 32-bit independent timer**
- **General DMA controller**
  - 7 channels. Support ring buffer management
  - Support peripherals: Timer/ADC/DAC/USART/I2C/SPI
- **12-bit DAC**
  - 2-channel analog signal output
- **12-bit ADC, 1us conversion time**
  - Conversion range: 0 to $V_{DDA}$
  - 16 external signal channels + 2 internal signal channels
  - On-chip temperature sensor
- **16-channel TouchKey detection**
- **7 timers**
  - 3 16-bit general-purpose timers, provide up to 4 channels for input capture/output comparison /PWM/pulse counting and incremental encoder input
  - A 16-bit advanced-control timer, has function of general-purpose timers, provides dead zone control and emergency brake, and provides PWM for motor control
  - 2 watchdog timers (independent watchdog and window watchdog)
  - System time timer: 24-bit self-increment counter

- **10 standard communication interfaces:**
  - USB2.0 FS device interface (full-speed and low-speed)
  - USB2.0 FS host/device interface (full-speed and low-speed)
  - 1 CAN interface (2.0B active)
  - 2 I2C interfaces (support SMBus/PMBus)
  - 3 USART interfaces (support ISO7816 interface, LIN, IrDA interface and modem control)
  - 2 SPI interfaces (support Master and Slave modes)
- **Fast GPIO ports**
  - 51 I/O ports, all mappable on 16 external interrupts
- **Security features:**

  CRC calculation unit, 96-bit unique ID
- **Debug mode:**

  Serial single-wire debug (SWD) interface
- **Package**
  - LQFP64M/LQFP48/QFN48X7

# Chapter 1 Specification information

CH32F1 series MCU products use high-performance 32-bit ARM®Cortex™-M3 RISC core. The highest operating frequency is 72MHz. A built-in high-speed memory is provided, and prefetching method is adopted to improve the command access speed. Multiple buses in the system structure work synchronously, providing abundant peripheral functions and enhanced I/O ports. This series of products have built-in functions such as a 12-bit ADC module, a 12-bit DAC module, 4 16-bit general-purpose timers, multi-channel capacitive touchkey detection (TKey), and also include standard communication interfaces: 2 I2C interfaces, 2 SPI interfaces, 3 USART interfaces, a CAN interface and 2 USB2.0 full-speed interfaces (full/low-speed communication).

The supply voltage range of this series of products is 2.7V～5.5V, and the operating temperature range is -40℃～85℃ industrial grade. They support a variety of power-saving operating modes to meet the low-power application requirements. The products in this series are different in terms of resource allocation, number of peripherals, peripheral functions, etc. You can choose according to your needs. Several packages forms are provided: LQFP64M/LQFP48/QFN48X7. It can be widely used in: motor drive and application control, medical and handheld devices, PC game peripherals and GPS platforms, programmable controllers, inverters, printers, scanners, alarm systems, video intercom, heating, ventilation and air conditioning systems, etc.

## 1.1 Comparison

Table1-1 CH32F103x product resource allocation

| Difference \ Product No. | | CH32F103 C6T6 | CH32F103 C8T6 | CH32F103 C8U6 | CH32F103 R8T6 |
|---|---|---|---|---|---|
| Pin count | | 48 | 48 | 48 | 64 |
| Flash (byte) | | 32K | 64K | 64K | 64K |
| SRAM (byte) | | 10K | 20K | 20K | 20K |
| GPIO port count | | 37 | 37 | 37 | 51 |
| Timer | General | 2 | 3 | 3 | 3 |
| | Advanced | 1 | 1 | 1 | 1 |
| | Watchdog | 2 | 2 | 2 | 2 |
| | SysTick | 1 | 1 | 1 | 1 |
| ADC/TKey (channel count) | | 10 | 10 | 10 | 16 |
| DAC channel count | | 2 | 2 | 2 | 2 |
| Communication interface | SPI | 1 | 2 | 2 | 2 |
| | I2C | 1 | 2 | 2 | 2 |
| | USART | 2 | 3 | 3 | 3 |
| | CAN | 1 | 1 | 1 | 1 |
| | USBD 2.0FS | 1 | 1 | 1 | 1 |
| | USBHD 2.0FS | 1 | 1 | 1 | 1 |
| CPU clock speed | | Max: 72MHz | | | |
| Operating voltage | | 2.7V～5.5V | | | |
| Operating temperature | | Industrial-grade: -40°C～85°C | | | |
| Package | | LQFP48 | | QFN48X7 | LQFP64M (10*10) |

## 1.2 System architecture

The CH32F1 is a microcontroller based on ARM®Cortex™-M3 core. The core, arbitration unit, DMA module and SRAM memory, etc. of the architecture interact through multiple sets of buses. The CH32F1 supports Flash access prefetch mechanism to speed up code execution. It is equipped with a general DMA controller to reduce the burden on the CPU and improve efficiency. The clock tree hierarchical management reduces the total operating power consumption of peripherals. At the same time, it also has a data protection mechanism and a clock security system protection mechanism to increase the system stability.

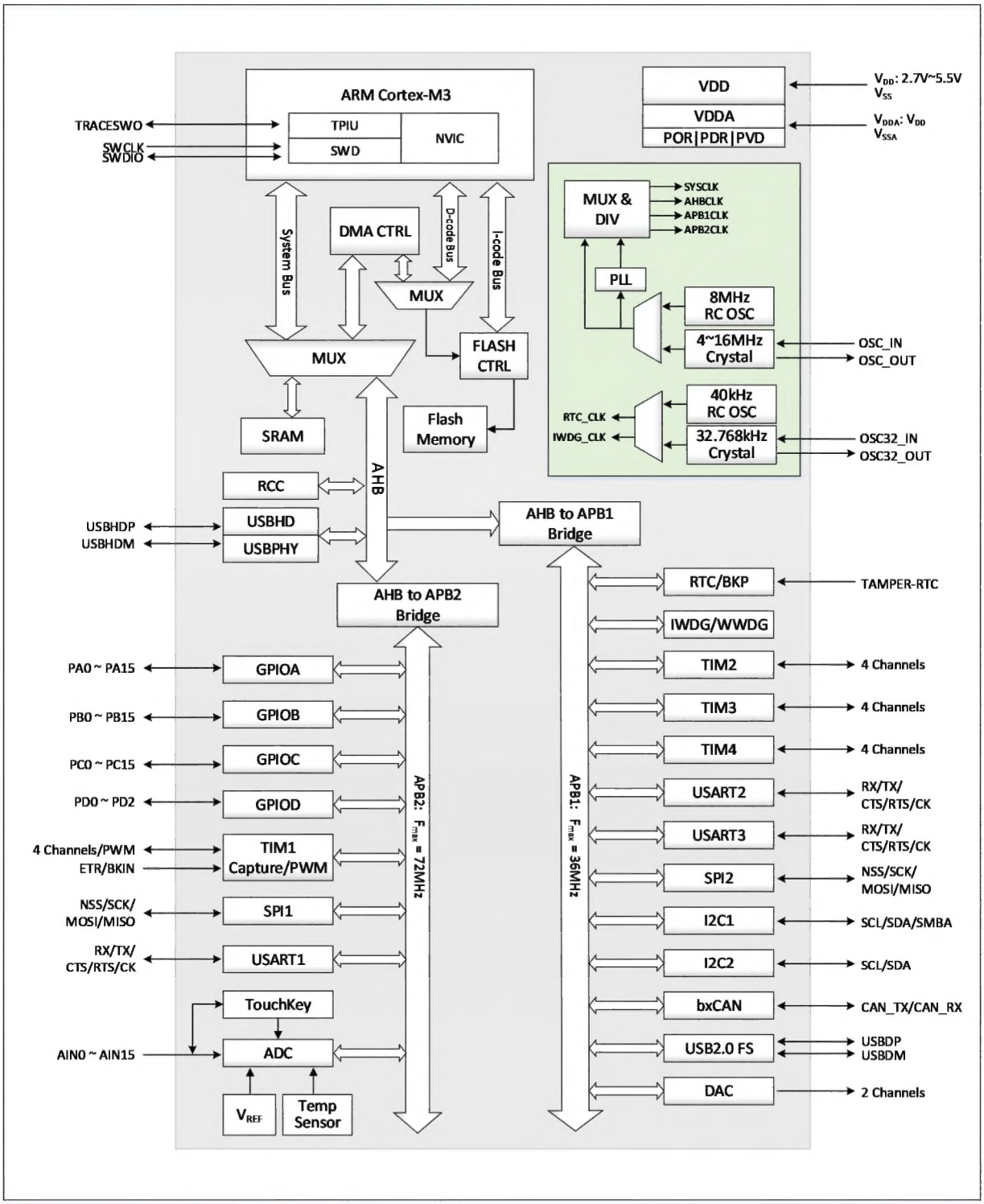


Figure 1-1 System architecture

## 1.3 Memory mapping

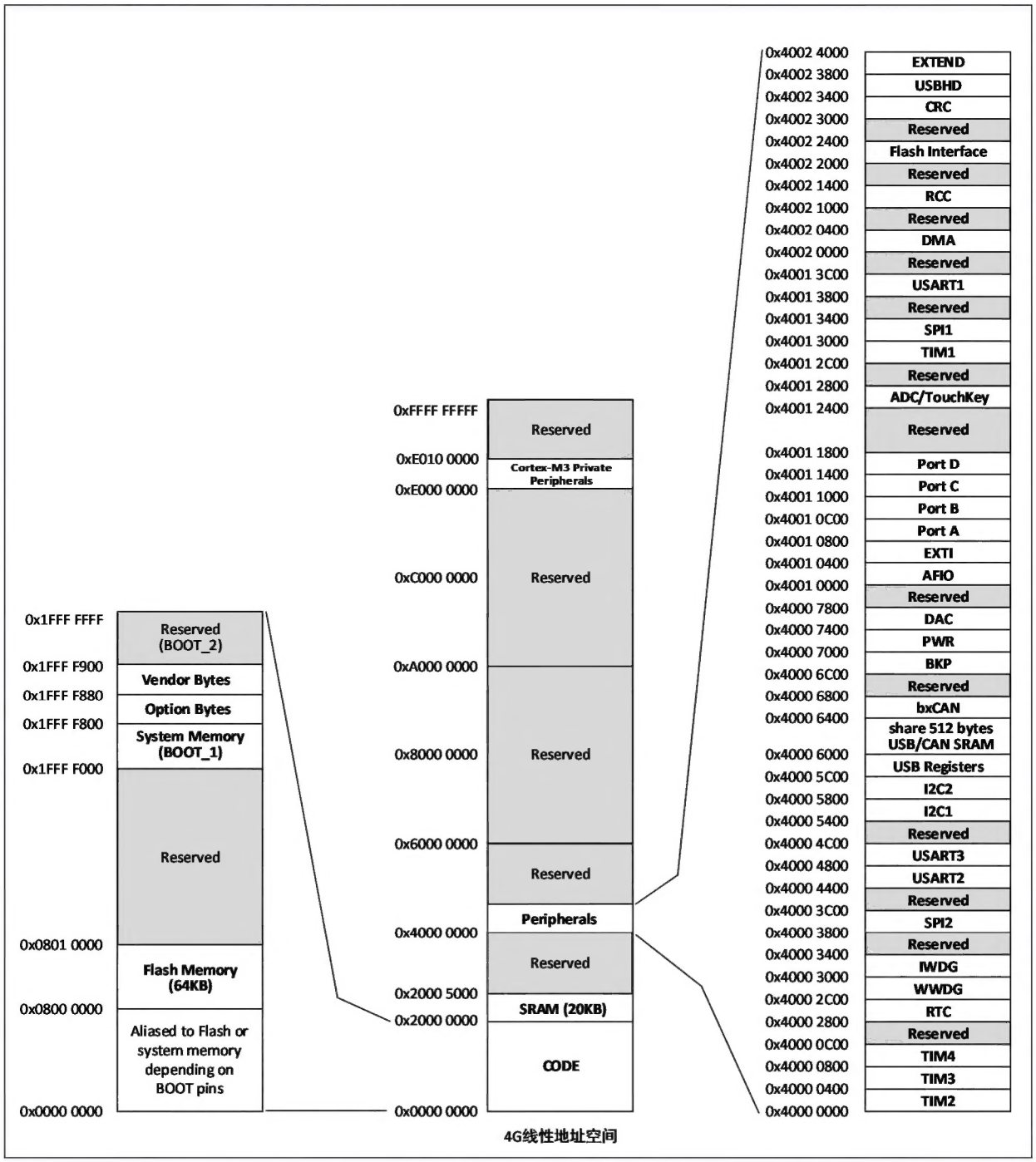


Figure 1-2 Memory address mapping

## 1.4 Clock tree

The system provides 4 sets of clock sources: high-speed internal RC oscillator (HSI), low-speed internal RC oscillator (LSI), high-speed external oscillator (HSE), and low-speed external oscillator (LSE). Among them, the system bus clock (SYSCLK) comes from a high-speed clock source or a higher clock generated by the PLL multiplier. And then AHB domain, APB1 domain, APB2 domain, timer and ADC sampling clock are configured by prescaler.

The low-speed clock source provides a clock reference for the RTC and independent watchdog.

The PLL multiplier clock provides the working clock reference of the USBD module and the USBHD module through the divider.

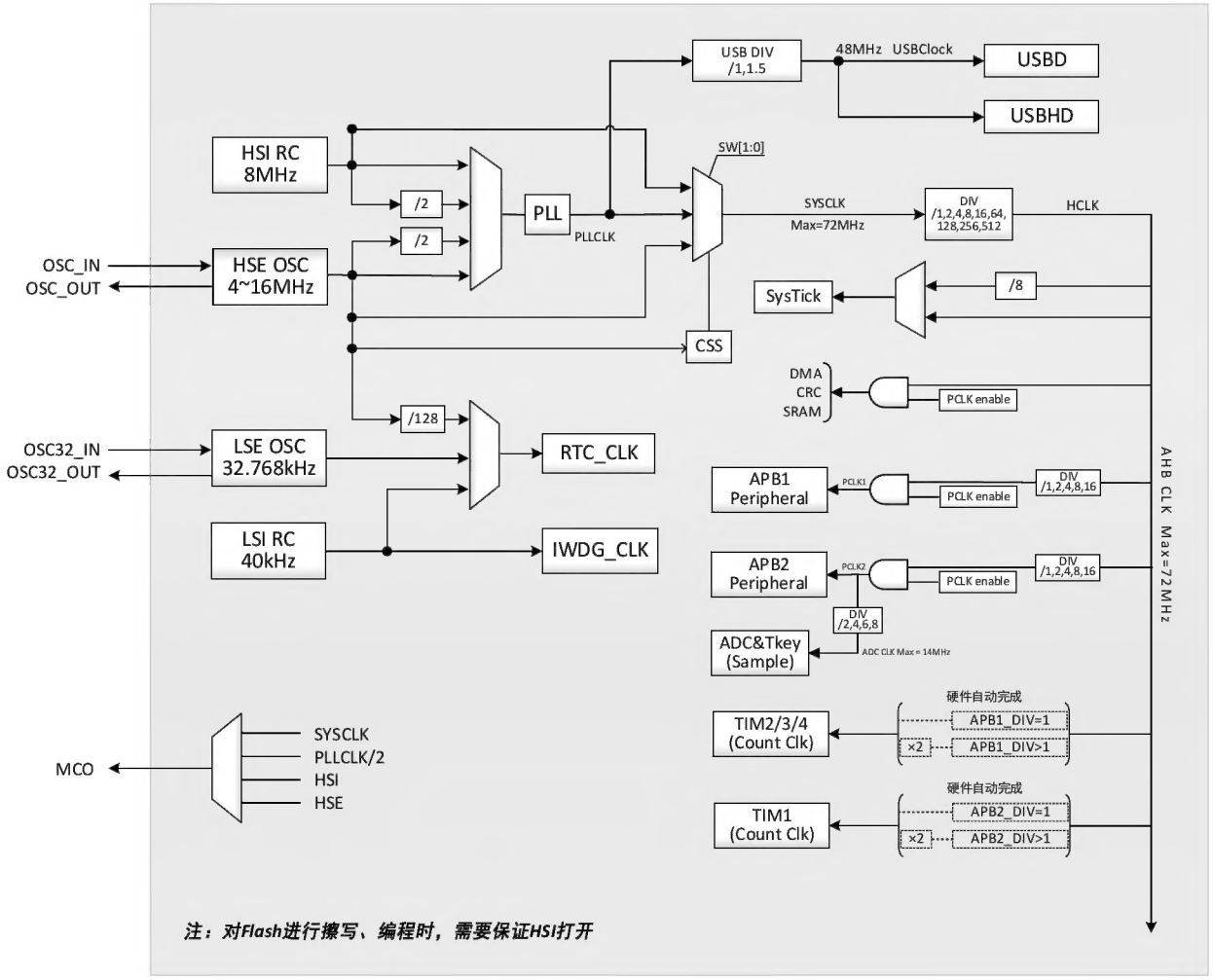


Figure 1-3 Clock tree block diagram

*Note:*

*When using USB function, HSE and PLL must be used simultaneously. The CPU clock speed must be 48MHz or 72MHz.*

*When the ADC sampling time is 1us, APB2 must be set to 14MHz or 28MHz or 56MHz.*

*When the system wakes up from sleep, the system automatically switches to HSI as the system clock frequency.*

*When performing erase/program operation on Flash, HSI must be turned on.*

## 1.5 Functional description

### 1.5.1 ARM®CortexTM-M3 core

ARM Cortex™-M3 is a 32-bit embedded processor. It provides low-cost platform, reduced pin count, low system power consumption, high computing performance and advanced interrupt system response to meet MCU requirements. Its extra code efficiency leverages the high performance of the ARM core over the memory space of typical 8- and 16-bit systems.

- Harvard architecture. Branch prediction function added, to improve pipeline processor performance play
- Interrupt tail-chaining mechanism, based on hardware, efficiency improved
- 3 low-power modes, more efficient to control power consumption
- Advanced Fault handling mechanism, debug solutions, etc.

The CH32F1 controller has a built-in ARM core, so it is compatible with most of ARM tools and software. Figure 1-1 shows the CH32F1 function block diagram.

### 1.5.2 On-chip memory and Boot mode

The built-in 20 Kbytes of SRAM area is used to store data.

The built-in 64 Kbytes of program flash storage area (CodeFlash) is used to store user application program.

The built-in 3.75 Kbytes of system storage area (BootLoader) is used to store system guidance program (manufacture's solidified boot loading program).

In addition, 128 bytes are used to store the manufacturer's configuration word, and 128 bytes are used to store the user select word.

During the startup, one of three bootstrap modes can be selected through the boot pins (BOOT0 and BOOT1):

- Boot from the program flash memory
- Boot from the system memory
- Boot from the internal SRAM

The boot loading program is saved in the system storage area and the contents of the program flash memory storage area can be re-programmed through the USART1 and USB interfaces.

### 1.5.3 Power supply scheme

- $V_{DD}$ = 2.7～5.5V: The $V_{DD}$ pin supplies power to I/O pins, RC oscillator, reset module and internal voltage regulator.
- $V_{DDA}$ = 2.7～5.5V: It supplies power to the simulation part of ADC, temperature sensor and PLL. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$ respectively.
- $V_{BAT}$ = 1.8～5.5V: When $V_{DD}$ is turned off, (through internal power switcher), it supplied power to RTC, external 32 KHz oscillator and backup register. (Note the supply of $V_{BAT}$)

### 1.5.4 Power supply supervisor

This product internally integrates a power-on reset (POR)/power-down reset (PDR) circuit, which is always in the working condition to ensure that the system works when the power supply exceeds 2.7V. When $V_{DD}$ is lower than the set threshold ($V_{POR/PDR}$), place the device in the reset state, and no external reset circuit is required.

In addition, there is a programmable voltage detector (PVD), which needs to be switched on by software to compare the voltage of $V_{DD}/V_{DDA}$ power supply and the set threshold $V_{PVD}$. Open the corresponding edge interrupt of PVD. When the $V_{DD}$ is reduced to PVD threshold or increased to PVD threshold, the interrupt notice will be received. Refer to Table 3-4 for the values of $V_{POR/PDR}$ and $V_{PVD}$.

### 1.5.5 Voltage regulator

After reset, the regulator will be automatically switched on. There are three operating modes according to the

application method.

- ON mode: The stable core power supply is provided through the normal operation
- Low power mode: After CPU enters Stop mode, you can select to operate the regulator at low power consumption
- OFF mode: When CPU enters Standby mode, the regulator is automatically switched to OFF mode, the voltage regulator output is in high impedance, and the core circuitry is powered down, inducing zero consumption.

The voltage regulator is always ON after reset. It is OFF in Standby mode, and the voltage regulator output is in high impedance.

### 1.5.6 Low-power mode

The CH32F1 supports 3 low power modes and can reach the optimum balance under the conditions of low power, short start time and multiple wake-up events.

- Sleep mode

Enter Sleep mode by executing WFI/WFE command. In Sleep mode, only the CPU clock stops, but the power supply of all peripheral clocks is normal and the peripherals are working. This mode is the shallowest low-power mode, but can reach the fastest wake-up.

Exit conditions: Any interrupt or wake-up event.

- Stop mode

Clear the PDDS bit. Set the SLEEPDEEP bit. Reset/set the LPDS bit. Enter Stop mode by executing WFI/WFE command. In Stop mode, FLASH enters low-power mode, and LPDS bit decides whether the core part is powered down, and the RC oscillator of PLL and HSI and HSE crystal oscillator are switched off. In Stop mode, the power consumption can reach the lowest when the contents of SRAM and register are maintained not to be lost.

Exit conditions: Any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset and a rising edge on WKUP pin. EXTI signals include one of 16 external I/O ports, PVD output, RTC clock and USB wake-up signal.

- Standby mode

Set the PDDS and SLEEPDEEP bits. Enter Standby mode by executing WFI/WFE command. The core part is powered down. The RC oscillator and HSE crystal oscillator of PLL and HSI are also switched off. The minimum power consumption can be achieved in this mode, but the system will reset after wake-up.

Exit conditions: Any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset and a rising edge on WKUP pin. EXTI signals include one of 16 external I/O ports, PVD output, RTC clock and USB wake-up signal.

### 1.5.7 Cyclic redundancy check (CRC) calculation unit

CRC (cyclic redundancy check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In many applications, CRC based technology is used to verify the consistency of data transfer and storage. Within the scope of EN/ IEC 60335-1 standard, a method of detecting flash memory error is provided. The CRC calculation unit can be used to calculate software signature real-timely and it shall be compared with the signature generated when linking and generating the software.

### 1.5.8 Nested vectored interrupt controller (NVIC)

The product has a built-in Nested Vectored Interrupt Controller (NVIC), which manages 44 maskable interrupt channels and 16 core interrupt channels. It has 16 programmable priority levels.

- Closely coupled NVIC, which enables low latency interrupt processing
- Vectorized interrupt design implements that vector entry address directly enters the core
- 16 nested levels, can be changed dynamically
- Enable early processing of interrupts
- Enable efficient processing of late arriving interrupts
- Support interrupt Tail-Chaining
- Provide first-time response to non-maskable interrupts
- Auto stack and resume during interrupt entry and exit, without additional instruction overhead

This module provides flexible interrupt management, with the lowest interrupt latency.

### 1.5.9 External interrupt/event controller (EXTI)

The external interrupt/event controller contains 20 edge detectors for generating interrupt/event requests. Each interrupt line can be configured independently to select the corresponding trigger event (rising or falling or both), and can be masked independently. The pending register maintains all interrupt request states. EXTI can detect the external signal with pulse width lower than internal APB2 clock period. Up to 51 general-purpose I/O ports can be selectively connected to 16 external interrupt lines.

### 1.5.10 General-purpose DMA controller

Flexible general-purpose DMA can manage the high-speed data transfer from memory to memory, peripheral to memory and memory to peripheral, providing 7 channels and supporting ring buffer area management. Each channel has special hardware DMA request logic, which supports the access request of one or more peripheral devices to the memory. The access priority, transfer length, source address and destination address of transmission can be configured.

The main peripherals used in DMA include: General-purpose/advanced-control timers Timer, ADC, DAC, USART, I2C and SPI.

### 1.5.11 Clock and startup

The system clock source HSI is on by default. After no clock is configured or reset, the internal 8MHz RC oscillator will be used as the default CPU clock, and then the external 4-16MHz clock or PLL clock can be selected. After the clock safety mode is switched on, if HSE is used as the system clock (directly or indirectly), the system clock will be automatically switched to the internal RC oscillator and HSE and PLL will be automatically turned off when the system detects the external clock failure; for the low power consumption mode of switching off the clock, the system will also automatically switch to the internal RC oscillator after wake-up. If the clock interrupt is enabled, the software can receive corresponding interrupt.

Several prescalers are used to configure AHB frequency, high-speed APB (APB2) and low-speed APB (APB1) area bus clock. Refer to Figure 1-2 Clock tree block diagram.

### 1.5.12 Real-time clock (RTC) and backup register

The RTC and backup register are in the backup power supply area inside the product. When the $V_{DD}$ is valid, the power will be supplied by the $V_{DD}$. Otherwise, the $V_{BAT}$ pin will be automatically switched internally to supply the power.

RTC real-time clock is a group of 32-bit programmable counters. The time base supports 20-bit prescaler, which is used for the measurement in the long period. The clock reference source is high-speed external clock divided by 128 (HSE/128), 32.768 KHz oscillator (LSE) of external crystal or internal low-power RC oscillator (LSI). The LSE also has a backup power supply area. Therefore, when LSE is selected as RTC time base, the setting and time of RTC can remain unchanged after the system is reset or woken up from the standby mode.

The backup register includes ten 16-bit registers, which can be used to store 20 bytes of user application data. The data can be maintained and will not be reset after the standby wake-up, or when the system is reset or the power is reset. When the intrusion detection function is switched on, once the intrusion detection signal is valid, all contents in the backup register can be cleared.

### 1.5.13 Analog-to-digital converter (ADC) and capacitive TouchKey detection (Tkey)

A 12-bit analog-to-digital converter (ADC) is embedded in the product, providing up to 16 external channels and 2 internal channels for sampling. For the programmable channel sampling time, single, continuous, scanning or intermittent modes conversion can be achieved. The analog watchdog function that allows very accurate monitoring of one or more selected channels is provided for monitoring the channel signal voltage. Supporting external event trigger conversion; the trigger sources include internal signal and external pin of on-chip timer (EXTI line 11). It supports DMA operation.

The ADC internal channel sampling includes 1-channel built-in temperature sensor sampling and 1-channel internal reference power sampling. The temperature sensor generates a voltage that varies linearly with temperature, and the power supply range is 3.0V <$V_{DDA}$ < 5.5V. The temperature sensor is internally connected to the ADC1_ IN16 input channel, used to convert the output of the sensor to a digital value.

The capacitive touch key detection unit provides up to 16 detection channels and multiplexes the external channel of ADC module. The detection result is output through ADC conversion, and the state of touch key can be identified by user software.

### 1.5.14 DAC (digital-to-analog converter)

A 12-bit digital-to-analog converter (DAC) is embedded in the product, which supports convert 2-channel digital signal to 2-channel analog voltage signal and output. It supports external triggers for conversion, and the trigger sources include the internal signal and external pin (EXTI line 9) of the on-chip timer. It also supports triangle-wave generation, noise-wave generation and DMA capability.

### 1.5.15 Timer

The timer consists of an advanced 16-bit timer, 3 general-purpose 16-bit timers, 2 watchdog timers and a system time base timer.

#### 1.5.15.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) is a 16-bit automatic loading counter with a programmable prescaler. In addition to the complete general timer function, it can be regarded as a three-phase PWM generator assigned to six channels, having the complementary PWM output function with dead zone insertion. The timer allows to be updated after a specified number of counter cycles for repeated counting cycle and braking function, etc. Many functions of advanced control timer are the same as those of general timer, and the internal structure is also the same. Therefore, advanced control timer can operate with TIM timer through timer link function to provide synchronization or event linking function.

#### 1.5.15.2 General-purpose timer (TIM2/3/4)

The system provides up to 3 standard timers (TIM2, TIM3 and TIM4) which can be operated synchronously. Each timer has a 16-bit auto-load increment/decrement counter, a programmable 16-bit prescaler and 4 independent channels, each of which can be used for input capture, output comparison, PWM generation and single pulse mode output.

It can also work with advanced-control timer through timer link function to provide synchronization or event linking function. In the debug mode, the counter can be frozen and the PWM output is disabled, thus switching off the switches controlled by these outputs. Any general-purpose timer can be used to generate PWM output. Each timer has its own DMA request mechanism.

These timers can also process signals from incremental encoders and digital outputs from 1 to 3 Hall sensors.

#### 1.5.15.3 Independent watchdog (IWDG)

The independent watchdog is a free running 12-bit down counter with an 8-bit prescaler. The clock is provided by an internally independent 40 KHz RC oscillator; since this RC oscillator is independent of the master clock, it can operate in stop and standby modes. IWDG completely works independently of the main program, so it can be used to reset the whole system in case of problems, or to provide timeout management for applications as a free timer. The option byte can be configured as a software or hardware boot watchdog. In the debug mode, the counter can be frozen.

#### 1.5.15.4 Window watchdog (WWDG)

The window watchdog is a 7-bit down counter and can be set to run freely. It can be used to reset the entire system in the event of a problem. It is driven by the master clock and has the function of early warning interrupt. In the debug mode, the counter can be frozen.

#### 1.5.15.5 System time base timer (SysTick)

This is a timer provided by the ARM core controller to generate SYSTICK exception (exception No. 15). It can be used in real-time operating system to provide "heartbeat" rhythm for the system. It can also be used as a standard 24-bit increment counter. It supports auto reload function and programmable clock source. When the counter reaches 0, a maskable system interrupt is generated.

### 1.5.16 Standard communication interface

#### 1.5.16.1 Universal synchronous asynchronous receiver transmitter (USART)

3 groups of USARTs support full duplex asynchronous communication, synchronous one-way communication,

half duplex single line communication and Lin (local Internet), and are compatible with ISO7816 smart card protocol, IrDA SIR ENDEC transfer encoder/decoder specifications, and modem (CTS/RTS hardware flow control) operation. The multi-processor communication is also supported. The fractional baud rate generator system is used. The baud rate of USART1 can be up to 4.5 Mbits/s, and baud rate of USART2/3 can be up to 2.25 Mbits/s. They support DMA operation for continuous communication.

#### 1.5.16.2 Serial peripheral interface (SPI)

2 sets of SPIs provide the master/slave operation and are switched dynamically. They support multi-master mode, full duplex or half duplex synchronous transfer, and support basic SD card and MMC mode. The clock frequency can be up to 36 MHz, clock polarity and phase are programmable, 8-bit or 16-bit data bit width can be selected, the hardware CRC generation/verification is reliable. They support DMA operation for continuous communication.

#### 1.5.16.3 I2C bus

Up to 2 I2C interfaces can work in multi-master mode and slave mode and can complete specific timing, protocol, arbitration, etc. for all I2C buses. They support standard communication speed and fast communication speed, and are compatible with SMBus2.0.

I2Cs provide 7-bit or 10-bit addressing, and support dual-slave addressing in 7-bit slave mode. The built-in hardware CRC generator/calibrator is provided. DMA operation can be used, SMBus2.0 and PMBus are supported.

#### 1.5.16.4 Controller area network (CAN)

The CAN interface supports the CAN protocols version 2.0A and 2.0B (active). The baud rate can be up to 1Mbits/s. It supports the Time Triggered Communication option. It can receive and transmit the standard frames with 11-bit identifiers, as well as receive and transmit the extended frames with 29-bit identifiers. It provides 3 transmit mailboxes, 2 receive FIFOs with three stages, and 14 scalable filter banks.

*Note: USBD and CAN share a dedicated 512-byte SRAM memory to receive and transmit data. When USBD and CAN are used concurrently, USBD can only use the lower 384-byte area, to avoid access to SRAM conflicted.*

#### 1.5.16.5 Universal serial bus (USB)

The product is embedded with 2 USB2.0 full-speed controllers, including a full-speed/low-speed USB device controller (USBD) and a full-speed/low-speed USB host/device controller (USBHD), which comply with USB2.0 Fullspeed Standard. USBD provides 16 configurable USB device endpoints and a set of host endpoint. It supports control/bulk/isochronous/interrupt transfer, double-buffered mechanism, USB Suspend/Resume operations, and provides standby/wake-up function. The dedicated 48 MHz clock of USBHD module is directly generated by internal main PLL divider (clock source must be HSE crystal oscillator).

### 1.5.17 General purpose input/output (GPIO)

The system provides 4 groups of GPIO ports with 51 GPIO pins in total. Each pin can be configured as an output (push-pull or open drain), an input (with or without pull-up or pull-down) or a multiplexed peripheral

function port by software. Most GPIO pins can be shared with digital or analog multiplexed peripherals. Except for the ports with analog input function, all GPIO pins have high current carrying capacity. It provides a locking mechanism to freeze IO configuration to avoid accidental writing to I/O register.

### 1.5.18 Serial single-wire debug interface (SWD)

The embedded ARM SW-DP interface is a serial single-wire debug interface. The SWDIO pin and the SWCLK pin are included.

# Chapter 2 Pinouts and pin definitions

## 2.1 Pinouts

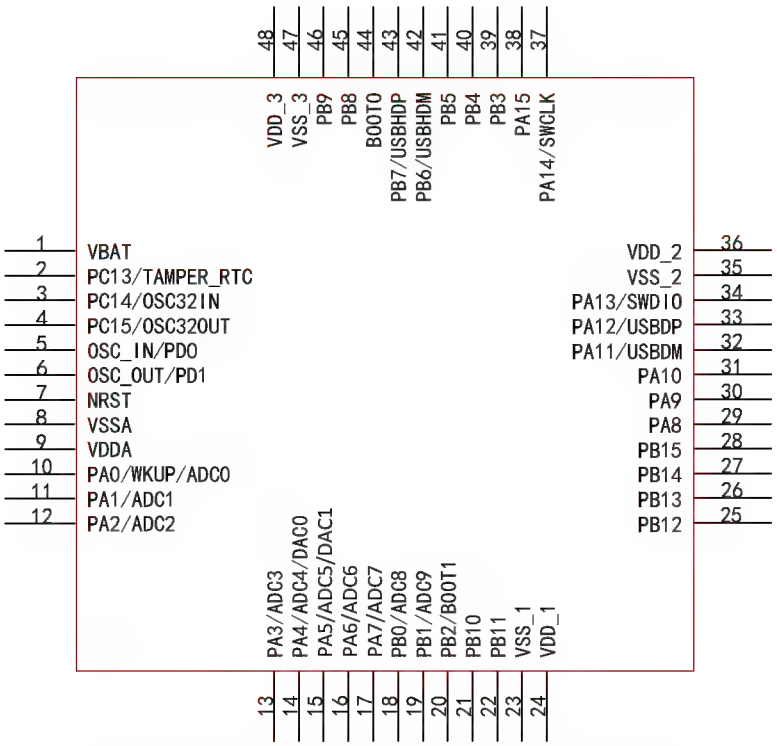


Figure 2-1 CH32F103Cx (LQFP48/QFN48X7) pinouts

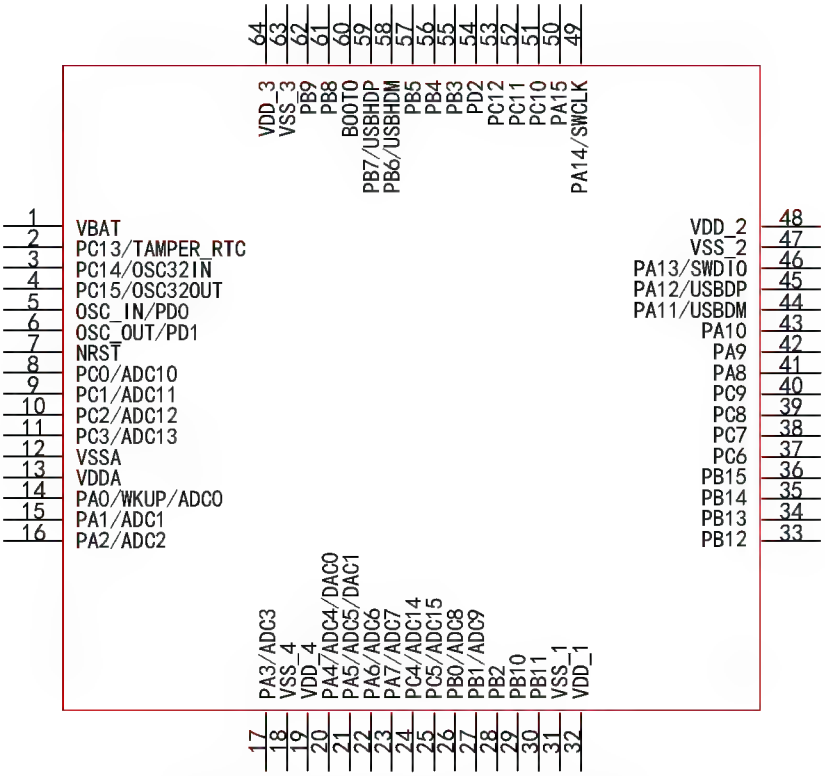


Figure 2-2 CH32F103Rx (LQFP64M) pinouts

## 2.2 Pin definitions

Table 2-1 CH32F103x8x6 pin definitions

| Pin No. | | | Pin Name | Pin Type | Main function (after reset) | Default alternate function | Remapping function |
|---|---|---|---|---|---|---|---|
| LQFP48 | QFN48X7 | LQFP64M | | | | | |
| 1 | 1 | 1 | $V_{BAT}$ | P | $V_{BAT}$ | | |
| 2 | 2 | 2 | PC13-TAMPER-RTC | I/O | PC13 | TAMPER-RTC | |
| 3 | 3 | 3 | PC14-OSC32_IN | I/O/A | PC14 | OSC32_IN | |
| 4 | 4 | 4 | PC15-OSC32_OUT | I/O/A | PC15 | OSC32_OUT | |
| 5 | 5 | 5 | OSC_IN | I/A | OSC_IN | | PD0 |
| 6 | 6 | 6 | OSC_OUT | O/A | OSC_OUT | | PD1 |
| 7 | 7 | 7 | NRST | I/O | NRST | | |
| - | - | 8 | PC0 | I/O/A | PC0 | ADC_IN10 | |
| - | - | 9 | PC1 | I/O/A | PC1 | ADC_IN11 | |
| - | - | 10 | PC2 | I/O/A | PC2 | ADC_IN12 | |
| - | - | 11 | PC3 | I/O/A | PC3 | ADC_IN13 | |
| 8 | 8 | 12 | $V_{SSA}$ | P | $V_{SSA}$ | | |
| 9 | 9 | 13 | $V_{DDA}$ | P | $V_{DDA}$ | | |
| 10 | 10 | 14 | PA0-WKUP | I/O/A | PA0 | WKUP/USART2_CTS/ADC_IN0 /TIM2_CH1/TIM2_ETR | |
| 11 | 11 | 15 | PA1 | I/O/A | PA1 | USART2_RTS/ADC_IN1 /TIM2_CH2 | |
| 12 | 12 | 16 | PA2 | I/O/A | PA2 | USART2_TX/ADC_IN2 /TIM2_CH3 | |
| 13 | 13 | 17 | PA3 | I/O/A | PA3 | USART2_RX/ADC_IN3 /TIM2_CH4 | |
| - | - | 18 | $V_{SS_4}$ | P | $V_{SS_4}$ | | |
| - | - | 19 | $V_{DD_4}$ | P | $V_{DD_4}$ | | |
| 14 | 14 | 20 | PA4 | I/O/A | PA4 | SPI1_NSS/USART2_CK /ADC_IN4/DAC_OUT1 | |
| 15 | 15 | 21 | PA5 | I/O/A | PA5 | SPI1_SCK/ADC_IN5 /DAC_OUT2 | |
| 16 | 16 | 22 | PA6 | I/O/A | PA6 | SPI1_MISO/ADC_IN6 /TIM3_CH1 | TIM1_BKIN |
| 17 | 17 | 23 | PA7 | I/O/A | PA7 | SPI1_MOSI/ADC_IN7 /TIM3_CH2 | TIM1_CH1N |
| - | - | 24 | PC4 | I/O/A | PC4 | ADC_IN14 | |
| - | - | 25 | PC5 | I/O/A | PC5 | ADC_IN15 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 18 | 18 | 26 | PB0 | I/O/A | PB0 | ADC_IN8/TIM3_CH3 | TIM1_CH2N |
| 19 | 19 | 27 | PB1 | I/O/A | PB1 | ADC_IN9/TIM3_CH4 | TIM1_CH3N |
| 20 | 20 | 28 | PB2 | I/O | PB2<br>/BOOT1 | | |
| 21 | 21 | 29 | PB10 | I/O | PB10 | I2C2_SCL/USART3_TX | TIM2_CH3 |
| 22 | 22 | 30 | PB11 | I/O | PB11 | I2C2_SDA/USART3_RX | TIM2_CH4 |
| 23 | 23 | 31 | $V_{SS_1}$ | P | $V_{SS_1}$ | | |
| 24 | 24 | 32 | $V_{DD_1}$ | P | $V_{DD_1}$ | | |
| 25 | 25 | 33 | PB12 | I/O | PB12 | SPI2_NSS/I2C2_SMBAI<br>/USART3_CK/TIM1_BKIN | |
| 26 | 26 | 34 | PB13 | I/O | PB13 | SPI2_SCK/USART3_CTS<br>/TIM1_CH1N | |
| 27 | 27 | 35 | PB14 | I/O | PB14 | SPI2_MISO/USART3_RTS<br>/TIM1_CH2N | |
| 28 | 28 | 36 | PB15 | I/O | PB15 | SPI2_MOSI/TIM1_CH3N | |
| - | - | 37 | PC6 | I/O | PC6 | | TIM3_CH1 |
| - | - | 38 | PC7 | I/O | PC7 | | TIM3_CH2 |
| - | - | 39 | PC8 | I/O | PC8 | | TIM3_CH3 |
| - | - | 40 | PC9 | I/O | PC9 | | TIM3_CH4 |
| 29 | 29 | 41 | PA8 | I/O | PA8 | USART1_CK/TIM1_CH1/MCO | |
| 30 | 30 | 42 | PA9 | I/O | PA9 | USART1_TX/TIM1_CH2 | |
| 31 | 31 | 43 | PA10 | I/O | PA10 | USART1_RX/TIM1_CH3 | |
| 32 | 32 | 44 | PA11 | I/O/A | PA11 | USART1_CTS/USBDM<br>/CAN_RX/TIM1_CH4 | |
| 33 | 33 | 45 | PA12 | I/O/A | PA12 | USART1_RTS/USBDP<br>/CAN_TX/TIM1_ETR | |
| 34 | 34 | 46 | PA13 | I/O | SWDIO | | PA13 |
| 35 | 35 | 47 | $V_{SS_2}$ | P | $V_{SS_2}$ | | |
| 36 | 36 | 48 | $V_{DD_2}$ | P | $V_{DD_2}$ | | |
| 37 | 37 | 49 | PA14 | I/O | SWCLK | | PA14 |
| 38 | 38 | 50 | PA15 | I/O | PA15 | | TIM2_CH1/TIM2_ETR<br>/SPI1_NSS |
| - | - | 51 | PC10 | I/O | PC10 | | USART3_TX |
| - | - | 52 | PC11 | I/O | PC11 | | USART3_RX |
| - | - | 53 | PC12 | I/O | PC12 | | USART3_CK |
| - | - | 54 | PD2 | I/O | PD2 | TIM3_ETR | |
| 39 | 39 | 55 | PB3 | I/O | PB3 | | TRACESWO<br>/TIM2_CH2/SPI1_SCK |
| 40 | 40 | 56 | PB4 | I/O | PB4 | | TIM3_CH1<br>/SPI1_MISO |
| 41 | 41 | 57 | PB5 | I/O | PB5 | I2C1_SMBAI | TIM3_CH2<br>/SPI1_MOSI |
| 42 | 42 | 58 | PB6 | I/O/A | PB6 | I2C1_SCL/TIM4_CH1/USBHDM | USART1_TX |
| 43 | 43 | 59 | PB7 | I/O/A | PB7 | I2C1_SDA/TIM4_CH2/USBHDP | USART1_RX |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 44 | 44 | 60 | BOOT0 | I | BOOT0 | | |
| 45 | 45 | 61 | PB8 | I/O/A | PB8 | TIM4_CH3 | I2C1_SCL/CAN_RX |
| 46 | 46 | 62 | PB9 | I/O/A | PB9 | TIM4_CH4 | I2C1_SDA/CAN_TX |
| 47 | 47 | 63 | $V_{SS_3}$ | P | $V_{SS_3}$ | | |
| 48 | 48 | 64 | $V_{DD_3}$ | P | $V_{DD_3}$ | | |

Table 2-2 CH32F103x6x6 pin definitions

| Pin No. | | Pin Name | Pin Type | Main function (after reset) | Default alternate function | Remapping function |
|---|---|---|---|---|---|---|
| LQFP48 | LQFP64M | | | | | |
| 1 | 1 | $V_{BAT}$ | P | $V_{BAT}$ | | |
| 2 | 2 | PC13-TAMPER-RTC | I/O | PC13 | TAMPER-RTC | |
| 3 | 3 | PC14-OSC32_IN | I/O/A | PC14 | OSC32_IN | |
| 4 | 4 | PC15-OSC32_OUT | I/O/A | PC15 | OSC32_OUT | |
| 5 | 5 | OSC8M_IN | I/A | OSC8M_IN | | PD0 |
| 6 | 6 | OSC8M_OUT | O/A | OSC8M_OUT | | PD1 |
| 7 | 7 | NRST | I/O | NRST | | |
| - | 8 | PC0 | I/O/A | PC0 | ADC_IN10 | |
| - | 9 | PC1 | I/O/A | PC1 | ADC_IN11 | |
| - | 10 | PC2 | I/O/A | PC2 | ADC_IN12 | |
| - | 11 | PC3 | I/O/A | PC3 | ADC_IN13 | |
| 8 | 12 | $V_{SSA}$ | P | $V_{SSA}$ | | |
| 9 | 13 | $V_{DDA}$ | P | $V_{DDA}$ | | |
| 10 | 14 | PA0-WKUP | I/O/A | PA0 | WKUP/USART2_CTS /ADC_IN0 /TIM2_CH1/TIM2_ETR | |
| 11 | 15 | PA1 | I/O/A | PA1 | USART2_RTS/ADC_IN1 /TIM2_CH2 | |
| 12 | 16 | PA2 | I/O/A | PA2 | USART2_TX/ADC_IN2 /TIM2_CH3 | |
| 13 | 17 | PA3 | I/O/A | PA3 | USART2_RX/ADC_IN3 /TIM2_CH4 | |
| - | 18 | $V_{SS_4}$ | P | $V_{SS_4}$ | | |
| - | 19 | $V_{DD_4}$ | P | $V_{DD_4}$ | | |
| 14 | 20 | PA4 | I/O/A | PA4 | SPI1_NSS/USART2_CK /ADC_IN4/DAC_OUT1 | |
| 15 | 21 | PA5 | I/O/A | PA5 | SPI1_SCK/ADC_IN5 /DAC_OUT2 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| 16 | 22 | PA6 | I/O/A | PA6 | SPI1_MISO/ADC_IN6 /TIM3_CH1 | TIM1_BKIN |
| 17 | 23 | PA7 | I/O/A | PA7 | SPI1_MOSI/ADC_IN7 /TIM3_CH2 | TIM1_CH1N |
| - | 24 | PC4 | I/O/A | PC4 | ADC_IN14 | |
| - | 25 | PC5 | I/O/A | PC5 | ADC_IN15 | |
| 18 | 26 | PB0 | I/O/A | PB0 | ADC_IN8/TIM3_CH3 | TIM1_CH2N |
| 19 | 27 | PB1 | I/O/A | PB1 | ADC_IN9/TIM3_CH4 | TIM1_CH3N |
| 20 | 28 | PB2 | I/O | PB2/BOOT1 | | |
| 21 | 29 | PB10 | I/O | PB10 | | TIM2_CH3 |
| 22 | 30 | PB11 | I/O | PB11 | | TIM2_CH4 |
| 23 | 31 | $V_{SS_1}$ | P | $V_{SS_1}$ | | |
| 24 | 32 | $V_{DD_1}$ | P | $V_{DD_1}$ | | |
| 25 | 33 | PB12 | I/O | PB12 | TIM1_BKIN | |
| 26 | 34 | PB13 | I/O | PB13 | TIM1_CH1N | |
| 27 | 35 | PB14 | I/O | PB14 | TIM1_CH2N | |
| 28 | 36 | PB15 | I/O | PB15 | TIM1_CH3N | |
| - | 37 | PC6 | I/O | PC6 | | TIM3_CH1 |
| - | 38 | PC7 | I/O | PC7 | | TIM3_CH2 |
| - | 39 | PC8 | I/O | PC8 | | TIM3_CH3 |
| - | 40 | PC9 | I/O | PC9 | | TIM3_CH4 |
| 29 | 41 | PA8 | I/O | PA8 | USART1_CK/TIM1_CH1 /MCO | |
| 30 | 42 | PA9 | I/O | PA9 | USART1_TX/TIM1_CH2 | |
| 31 | 43 | PA10 | I/O | PA10 | USART1_RX/TIM1_CH3 | |
| 32 | 44 | PA11 | I/O/A | PA11 | USART1_CTS/USBDM /CAN_RX/TIM1_CH4 | |
| 33 | 45 | PA12 | I/O/A | PA12 | USART1_RTS/USBDP /CAN_TX/TIM1_ETR | |
| 34 | 46 | PA13 | I/O | SWDIO | | PA13 |
| 35 | 47 | $V_{SS_2}$ | P | $V_{SS_2}$ | | |
| 36 | 48 | $V_{DD_2}$ | P | $V_{DD_2}$ | | |
| 37 | 49 | PA14 | I/O | SWCLK | | PA14 |
| 38 | 50 | PA15 | I/O | PA15 | | TIM2_CH1/TIM2_ETR /SPI1_NSS |
| - | 51 | PC10 | I/O | PC10 | | |
| - | 52 | PC11 | I/O | PC11 | | |
| - | 53 | PC12 | I/O | PC12 | | |
| - | 54 | PD2 | I/O | PD2 | TIM3_ETR | |
| 39 | 55 | PB3 | I/O | PB3 | | TRACESWO/TIM2_CH2 /SPI1_SCK |
| 40 | 56 | PB4 | I/O | PB4 | | TIM3_CH1/SPI1_MISO |
| 41 | 57 | PB5 | I/O | PB5 | I2C1_SMBAI | TIM3_CH2/SPI1_MOSI |

| | | | | | | |
|---|---|---|---|---|---|---|
| 42 | 58 | PB6 | I/O/A | PB6 | I2C1_SCL/USBHDM | USART1_TX |
| 43 | 59 | PB7 | I/O/A | PB7 | I2C1_SDA/USBHDP | USART1_RX |
| 44 | 60 | BOOT0 | I | BOOT0 | | |
| 45 | 61 | PB8 | I/O/A | PB8 | | I2C1_SCL/CAN_RX |
| 46 | 62 | PB9 | I/O/A | PB9 | | I2C1_SDA/CAN_TX |
| 47 | 63 | $V_{SS_3}$ | P | $V_{SS_3}$ | | |
| 48 | 64 | $V_{DD_3}$ | P | $V_{DD_3}$ | | |

*Note: Pin Type:*

*I = TTL/CMOS Schmitt input;*

*O = CMOS three-state output;*

*A = Analog signal input or output;*

*P = Power.*

# Chapter 3 Electrical characteristics

## 3.1 Test conditions

Unless otherwise specified and indicated, all voltages are referenced to $V_{SS}$.

All minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency. Typical values are based on the normal temperature and $V_{DD}$ = 3.3V, and they are given only as design guidelines.

Data based on characterization results, design simulation or technology characteristics are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests.

Normal temperature: 25°C
Power supply scheme:

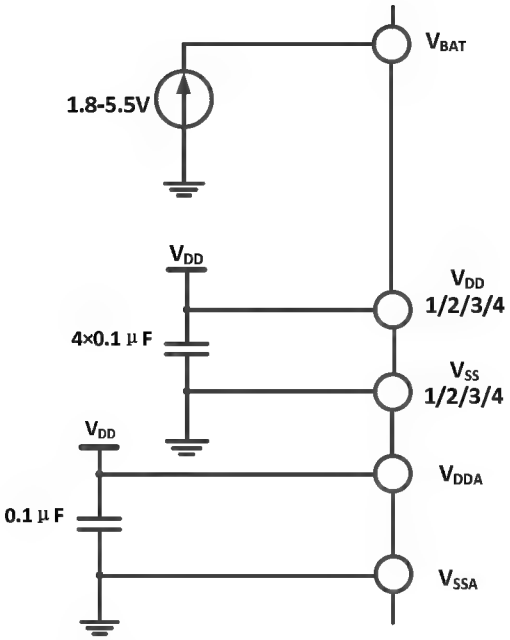


Figure 3-1 Power supply scheme

## 3.2 Absolute maximum ratings

Operating in critical ratings or exceeding the absolute maximum ratings may cause the chip to work abnormally or even be damaged.

Table 3-1 Absolute maximum ratings

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_A$[1] | Operating ambient temperature | -40 | 85 | ℃ |
| $T_S$ | Storage ambient temperature | -40 | 105 | ℃ |
| $V_{DD}$-$V_{SS}$[1] | External main supply voltage (including $V_{DDA}$ and $V_{DD}$) | -0.3 | 5.5 | V |
| $V_{IN}$[1] | Input voltage on pins | $V_{SS}$-0.3 | 5.5 | V |
| $\lvert\triangle V_{DDx}\rvert$[1] | Variations between different power pins | | 50 | mV |
| $\lvert V_{SSx}$-$V_{SS}\rvert$[1] | Variations between different ground pins | | 50 | mV |

| | | | | |
|---|---|---|---|---|
| $V_{ESD(HBM)}$[1] | ESD voltage (human body model, non-contact type) | 4000 | | V |
| $I_{VDD}$[2] | Total current into $V_{DD}/V_{DDA}$ power lines (source) | | 50 | mA |
| $I_{Vss}$[2] | Total current out of $V_{SS}$ ground lines (sink) | | 50 | |
| $I_{IO}$[1] | Output current sunk by any I/O and control pin | | 25 | |
| | Output current on any I/O and control pin | | -25 | |

*Notes: 1. Parameters are guaranteed by design.*

*2. The maximum current value can be reached in normal operation.*

## 3.3 Electrical characteristics

### 3.3.1 Operating conditions

Table 3-2 General operating conditions

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $F_{HCLK}$ | Internal AHB clock frequency | | | 72 | MHz |
| $F_{PCLK1}$ | Internal APB1 clock frequency | | | 36 | MHz |
| $F_{PCLK2}$ | Internal APB2 clock frequency | | | 72 | MHz |
| $V_{DD}$ | Standard operating voltage | | 2.7 | 5.5 | V |
| $V_{DDA}$ | Analog operating voltage (ADC is not used) | Must be the same potential as $V_{DD}$. | 2.7 | 5.5 | V |
| | Analog operating voltage (ADC is used) | | 3.0 | | |
| $V_{BAT}$[2] | Backup operating voltage | Cannot be more than $V_{DD}$ | 1.8 | 5.5 | V |
| $T_A$[1] | Ambient temperature | | -40 | 85 | °C |

*Notes: 1. Parameters are guaranteed by design.*

*2. The connecting line from the battery to $V_{BAT}$ shall be as short as possible.*

Table 3-3 Operating conditions at power-on / power-down

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | | 0 | ∞ | us/V |
| | $V_{DD}$ fall time rate | | 50 | ∞ | us/V |

*Note: The connecting line from the battery to $N_{BAT}$ shall be as short as possible.*

### 3.3.2 Embedded reset and power control block characteristics

Table 3-4 Reset and voltage monitor

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$[2] | Programmable voltage detector level selection | PLS[2:0] = 000 (rising edge) | | 2.65 | | V |
| | | PLS[2:0] = 000 (falling edge) | | 2.5 | | V |
| | | PLS[2:0] = 001 (rising edge) | | 2.87 | | V |
| | | PLS[2:0] = 001 (falling edge) | | 2.7 | | V |
| | | PLS[2:0] = 010 (rising edge) | | 3.07 | | V |
| | | PLS[2:0] = 010 (falling edge) | | 2.89 | | V |
| | | PLS[2:0] = 011 (rising edge) | | 3.27 | | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | PLS[2:0] = 011 (falling edge) | | 3.08 | | V |
| | | PLS[2:0] = 100 (rising edge) | | 3.46 | | V |
| | | PLS[2:0] = 100 (falling edge) | | 3.27 | | V |
| | | PLS[2:0] = 101 (rising edge) | | 3.76 | | V |
| | | PLS[2:0] = 101 (falling edge) | | 3.55 | | V |
| | | PLS[2:0] = 110 (rising edge) | | 4.07 | | V |
| | | PLS[2:0] = 110 (falling edge) | | 3.84 | | V |
| | | PLS[2:0] = 111 (rising edge) | | 4.43 | | V |
| | | PLS[2:0] = 111 (falling edge) | | 4.18 | | V |
| $V_{PVDhyst}$[1] | PVD hysteresis | | | 0.2 | | V |
| $V_{POR/PDR}$[1] | Power-on/power-down reset threshold | Rising edge | | 2.5 | | V |
| | | Falling edge | | 2.42 | | V |
| $V_{PDRhyst}$[1] | PDR hysteresis | | 40 | | 110 | mV |
| $t_{RSTTEMPO}$[1] | Reset temporization | | 16 | | 44 | mS |

*Notes: 1. Parameters are guaranteed by design.*

*2. Parameters are tested and based on the normal temperature.*

### 3.3.3 Internal reference voltage

Table 3-5 Internal reference voltage

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | $T_A$ = -40°C～85°C | 1.12 | 1.28 | V |
| $T_{S_vrefint}$ | Sample time of ADC when reading out internal reference voltage | | 0.107 | 17.1 | us |

### 3.3.4 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, product software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed code, etc.

The current consumption is measured as shown in the figure below:

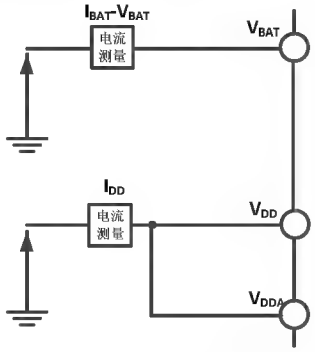


Figure 3-2 Current consumption measurement scheme

The MCU is placed under the following conditions:

Based on normal temperature, $V_{DD}$ = 3.3V, and all IO ports are configured as pull-up inputs, all peripheral

clocks (excluding GPIO peripherals) are enabled or disabled, and peripheral functions are not initialized.

Table 3-6 Typical current consumption in Run mode, code with data processing running from internal flash memory

| Symbol | Parameter | Condition | | Typ. | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled | All peripherals disabled | |
| $I_{DD}$ | Supply current in Run mode | External clock | $F_{HCLK}$ = 72MHz | 16.24 | 12.75 | mA |
| | | | $F_{HCLK}$ = 48MHz | 11.57 | 9.26 | |
| | | | $F_{HCLK}$ = 36MHz | 9.63 | 7.98 | |
| | | | $F_{HCLK}$ = 24MHz | 7.58 | 5.94 | |
| | | | $F_{HCLK}$ = 16MHz | 5.53 | 4.64 | |
| | | | $F_{HCLK}$ = 8MHz | 3.50 | 2.97 | |
| | | | $F_{HCLK}$ = 4MHz | 2.64 | 2.40 | |
| | | | $F_{HCLK}$ = 500KHz | 2.04 | 2.01 | |
| | | Run in high-speed internal RC oscillator (HSI), and use AHB prescaler to reduce frequency | $F_{HCLK}$ = 64MHz | 14.17 | 11.08 | |
| | | | $F_{HCLK}$ = 48MHz | 11.16 | 8.72 | |
| | | | $F_{HCLK}$ = 36MHz | 8.77 | 6.98 | |
| | | | $F_{HCLK}$ = 24MHz | 6.45 | 5.26 | |
| | | | $F_{HCLK}$ = 16MHz | 4.93 | 4.13 | |
| | | | $F_{HCLK}$ = 8MHz | 2.95 | 2.57 | |
| | | | $F_{HCLK}$ = 4MHz | 2.19 | 2.00 | |
| | | | $F_{HCLK}$ = 500KHz | 1.52 | 1.50 | |

*Note: The parameters above are actually measured.*

Table 3-7 Typical current consumption in Sleep mode, code with data processing running from internal flash memory or SRAM

| Symbol | Parameter | Condition | | Typ. | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled | All peripherals disabled | |
| $I_{DD}$ | Supply current in Sleep mode (In this case, peripheral power supply and clock are maintained) | External clock | $F_{HCLK}$ = 72MHz | | | 9.96 |
| | | | $F_{HCLK}$ = 48MHz | 7.32 | 4.55 | |
| | | | $F_{HCLK}$ = 36MHz | 6.34 | 4.29 | |
| | | | $F_{HCLK}$ = 24MHz | 5.16 | 3.49 | |
| | | | $F_{HCLK}$ = 16MHz | 4.14 | 3.16 | |
| | | | $F_{HCLK}$ = 8MHz | 2.68 | 2.21 | |
| | | | $F_{HCLK}$ = 4MHz | 2.34 | 2.04 | |
| | | | $F_{HCLK}$ = 500KHz | 1.93 | 1.89 | |
| | | Run in high-speed internal RC oscillator (HSI), and use | $F_{HCLK}$ = 64MHz | 8.80 | 4.95 | |
| | | | $F_{HCLK}$ = 48MHz | 7.06 | 4.16 | |
| | | | $F_{HCLK}$ = 36MHz | 5.73 | 3.56 | |
| | | | $F_{HCLK}$ = 24MHz | 4.42 | 2.96 | |
| | | | $F_{HCLK}$ = 16MHz | 3.60 | 2.63 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | AHB prescaler to reduce frequency | $F_{HCLK}$ = 8MHz | 2.30 | 1.82 | |
| | | | $F_{HCLK}$ = 4MHz | 1.90 | 1.66 | |
| | | | $F_{HCLK}$ = 500KHz | 1.54 | 1.52 | |

*Note: The parameters above are actually measured.*

Table 3-8 Typical current consumption in Stop and Standby modes

| Symbol | Parameter | Condition | Typ. | Unit |
|---|---|---|---|---|
| $I_{DD}$ | Supply current in Stop mode | The voltage regulator is in Run mode, and the low-speed and high-speed internal RC oscillators and external oscillators are off (no independent watchdog) | 455 | uA |
| | | The voltage regulator is in low power mode, and the low-speed and high-speed internal RC oscillators and external oscillators are off (no independent watchdog) | 2.3 | |
| | Supply current in Standby mode | Low-speed internal RC oscillator and independent watchdog are on | 3.3 | |
| | | The low-speed internal RC oscillator is on, and the independent watchdog is off. | 3.1 | |
| | | The low-speed internal RC oscillator and the independent watchdog are off. The low-speed external oscillator and RTC are off. | 2.3 | |
| $I_{DD_VBAT}$ | Backup domain supply current ($V_{DD}$ and $V_{DDA}$ are removed, and only $V_{BAT}$ is used to supply power) | Low-speed external oscillator and RTC are on | 2.5 | |

*Note: The parameters above are actually measured.*

### 3.3.5 External clock source characteristics

Table 3-9 From external high-speed clock

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{HSE_ext}$ | External clock frequency | | | 8 | 25 | MHz |
| $V_{HSEH}$[1] | OSC_IN input pin high level voltage | | $0.8V_{DD}$ | | $V_{DD}$ | V |
| $V_{HSEL}$[1] | OSC_IN input pin low level voltage | | 0 | | $0.2V_{DD}$ | V |
| $C_{in(HSE)}$ | OSC_IN input capacitance | | | 5 | | pF |
| $DuCy_{(HSE)}$ | Duty cycle | | | 50 | | % |

*Note: 1. Failure to meet this condition may cause level recognition errors.*

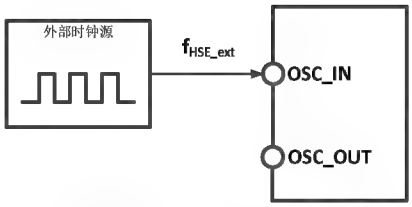


Figure 3-3 High-speed external clock scheme

Table 3-10 From external low-speed clock

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{LSE_ext}$ | External user clock source frequency | | | 32.768 | 1000 | KHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.8V_{DD}$ | | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | 0 | | $0.2V_{DD}$ | V |
| $C_{in(LSE)}$ | OSC32_IN input capacitance | | | 5 | | pF |
| $DuCy_{(LSE)}$ | Duty cycle | | | 50 | | % |

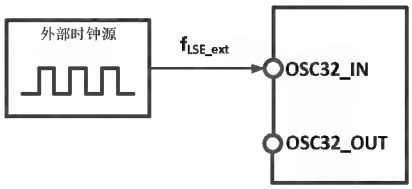


Figure 3-4 Low-speed external clock source scheme

Table 3-11 High-Speed external clock generated from a crystal/ceramic resonator

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{OSC_IN}$ | Oscillator frequency | | 4 | 8 | 16 | MHz |
| $I_2$[1] | HSE driving current | $V_{DD}$ = 3.3V, 20p load | | 0.2 | | mA |
| $g_m$[1] | Oscillator transconductance | Startup | | 4.6 | | mA/V |
| $t_{SU(HSE)}$ | Startup time | V DD is stabilized | | 1 | | ms |

*Note: 1. Parameters are guaranteed by design.*

Reference scheme and requirements:

The capacitance of the selected load crystal is generally 20pF ($C_{L1}$=$C_{L2}$, recommended 5~25pF). Please refer to the datasheet of the selected crystal.

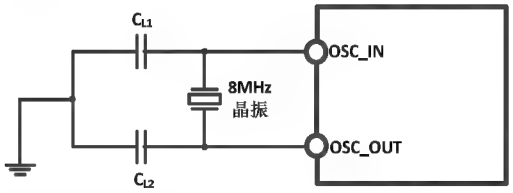


Figure 3-5 Typical application with an external 8 MHz crystal

Table 3-12 Low-speed external clock generated from a crystal/ceramic resonator ($f_{(LSE)}$=32.768KHz)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $i_2$[1] | LSE driving current | $V_{DD}$ = 3.3V | | 0.5 | | uA |

| | | | | | | |
|---|---|---|---|---|---|---|
| $g_m$[1] | Oscillator transconductance | Startup | | 13.5 | | uA/V |
| $t_{SU(LSE)}$ | Startup time | V DD is stabilized | | 200 | | mS |

*Note: 1. Parameters are guaranteed by design.*

Reference scheme and requirements:

The capacitance of the selected load crystal generally shall not exceed 15pF ($C_{L1}$ =$C_{L2}$ , recommended 5~15pF). Please refer to the datasheet of the selected crystal.

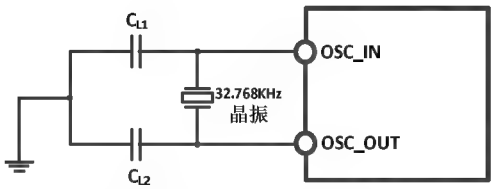


Figure 3-6 Typical application with an external 32.768 KHz crystal

*Note: The load capacitance $C_L$ is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, whereof $C_{stray}$ is the capacitance of the pin and the related capacitance of PCB board or PCB. Its typical value is between 2pF and 7pF.*

### 3.3.6 Internal clock source characteristics

Table 3-13 High-speed internal (HSI) RC oscillator characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{HSI}$ | Frequency | | | 8 | | MHz |
| $DuCy_{HSI}$ | Duty cycle | | 45 | 50 | 55 | % |
| $ACC_{HSI}$ | Accuracy of HSI oscillator | $T_A$ = 0℃~70℃ | -1.8 | | 1.8 | % |
| | | $T_A$ = -40℃~85℃ | -3 | | 2.5 | % |
| $t_{SU(HSI)}$ | HSI oscillator startup time | | | | 2.6 | us |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | | 200 | | uA |

Table 3-14 Low-speed internal (LSI) RC oscillator characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{LSI}$ | Frequency | | 25 | 36 | 60 | KHz |
| $DuCy_{LSI}$ | Duty cycle | | 45 | 50 | 55 | % |
| $t_{SU(LSI)}$ | LSI oscillator startup time | | | | 82 | us |
| $I_{DD(LSI)}$[1] | LSI oscillator power consumption | | | 0.6 | | uA |

*Note: 1. Parameters are guaranteed by design.*

### 3.3.7 PLL characteristics

Table 3-15 PLL characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{PLL\ IN}$ | PLL input clock | | 4 | 8 | 16 | MHz |
| | PLL input clock duty cycle [1] | | 40 | | 60 | % |

| | | | | | | |
|---|---|---|---|---|---|---|
| $F_{PLL_OUT}$ | PLL multiplier output clock | | | | 72 | MHz |
| $t_{LOCK}$[1] | PLL lock time | | | | 1000 | $1/F_{PLL_IN}$ |

*Note: 1. Parameters are guaranteed by design.*

### 3.3.8 Time to wake up from low-power mode

Table 3-16 Time to wake up from low-power mode

| Symbol | Parameter | Condition | Typ. | Unit |
|---|---|---|---|---|
| $t_{wusleep}$ | Wake up from Sleep mode | The clock source is the HSI RC oscillator | 6.84 | us |
| $t_{wustop}$ | Wake up from Stop mode (voltage regulator is in Run mode) | The clock source is the HSI RC oscillator | 261 | us |
| | Wake up from the stop mode (voltage regulator is in low-power mode) | Time to wake regulator up from low-power mode + HSI RC clock wake-up + flash startup | 261 | us |
| $t_{WUSTDBY}$ | Wake up from Standby mode | Time to wake regulator up from low-power mode + HSI RC clock wake-up + flash start | 440 | us |

### 3.3.9 Memory characteristics

Table 3-17 Flash memory characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{ERASE_128}$ | Page (128 bytes) programming time | $T_A$ = -40°C～85°C | 2.5 | 2.75 | 3 | ms |
| $t_{ERASE}$ | Page (128 bytes) erase time | $T_A$ = -40°C～85°C | 2.5 | 2.75 | 3 | ms |
| $t_{prog}$ | 16-bit programming time | $T_A$ = -40°C～85°C | 2.5 | 2.75 | 3 | ms |
| $t_{ERASE}$ | Page (1 Kbytes) erase time | $T_A$ = -40°C～85°C | 20 | 22 | 24 | ms |
| $t_{ME}$ | Mass erase time | $T_A$ = -40°C～85°C | 2.5 | 2.75 | 3 | ms |
| $V_{prog}$ | Programming voltage | | 2.7 | | 5.5 | V |

Table 3-18 Flash memory endurance and data retention

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $N_{END}$ | Endurance | $T_A$ = 25°C | 10K | 80K[1] | | cycles |
| $t_{RET}$ | Data retention | | 10 | | | years |

*Note: The value of endurance is actually measured, not guaranteed.*

### 3.3.10 I/O port characteristics

Table 3-19 General-purpose I/O static characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | TTL ports | -0.3 | | 0.8 | V |
| $V_{IH}$ | Standard I/O pin, input high | TTL ports 2.7V<$V_{DD}$<4.2V | 2 | | $V_{DD}$+0.3 | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | level voltage | TTL ports 4.2V≤$V_{DD}$<5.5V | 0.55$V_{DD}$ | | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input low level voltage | CMOS ports | -0.3 | | 0.8 | V |
| $V_{IH}$ | Input high level voltage | | 0.65$V_{DD}$ | | $V_{DD}$+0.3 | V |
| $V_{hys}$ | Schmitt trigger voltage hysteresis for standard I/O pin | | | 330 | | mV |
| $I_{lkg}$ | Input leakage current | | | | ±1 | uA |
| $R_{PU}$ | Weak pull-up equivalent resistance | | 30 | 42 | 55 | KΩ |
| $R_{PD}$ | Weak pull-down equivalent resistance | | 30 | 42 | 55 | KΩ |
| $C_{IO}$ | I/O pin capacitance | | | 5 | | pF |

*Note: The parameters are guaranteed by design.*

Output driving current characteristics

The GPIOs (general-purpose input/outputs) can sink or source up to ±8mA, and sink or source up to ±20mA (with a relaxed $V_{OL}$/$V_{OH}$). In the user applications, the sum of the currents sourced by all the IO pins cannot exceed the absolute maximum ratings provided in Section 3.2:

Table 3-20 Output voltage characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level, single-pin sunk | TTL ports, $I_{IO}$= +8mA | | 0.4 | V |
| $V_{OH}$ | Output high level, single pin sourced | 2.7V< $V_{DD}$ <5.5V | $V_{DD}$-0.4 | | V |
| $V_{OL}$ | Output low level, single-pin sunk | CMOS ports, $I_{IO}$= +8mA | | 0.4 | V |
| $V_{OH}$ | Output high level, single pin sourced | 2.7V< $V_{DD}$ <5.5V | 2.3 | | V |
| $V_{OL}$ | Output low level, single-pin sunk | $I_{IO}$= +20mA | | 1.3 | V |
| $V_{OH}$ | Output high level, single pin sourced | 2.7V< $V_{DD}$ <5.5V | $V_{DD}$-1.3 | | V |

*Note: In the above conditions, if several IO pins are driven at the same time, the sum of the currents cannot exceed the absolute maximum ratings given in Section 3.2. In addition, when several IO pins are driven at the same time, the currents on the power/ground lines are large, which will result in the voltage drop to make the internal IO voltage not reach the supply voltage listed in the table, causing the drive current to be less than the nominal value.*

Table 3-21 Input/output AC characteristics

| MODEx[1:0] configuration | Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| 10 (2MHz) | $F_{max(IO)out}$ | Maximum frequency | CL=50pF,VDD=2.7-5.5V | | 2 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | CL=50pF,VDD=2.7-5.5V | | 125 | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | | 125 | ns |
| 01 (10MHz) | $F_{max(IO)out}$ | Maximum frequency | CL=50pF,VDD=2.7-5.5V | | 10 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | CL=50pF,VDD=2.7-5.5V | | 25 | ns |

| | | | | | | |
|---|---|---|---|---|---|---|
| | $t_{r(IO)out}$ | Output low to high level rise time | | | 25 | ns |
| 11 (50MHz) | $F_{max(IO)out}$ | Maximum frequency | CL=30pF,VDD=2.7-5.5V | | 50 | MHz |
| | | | CL=50pF,VDD=2.7-5.5V | | 30 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | CL=30pF,VDD=2.7-5.5V | | 20 | ns |
| | | | CL=50pF,VDD=2.7-5.5V | | 5 | ns |
| | $t_{r(IO)out}$ | Output high to low level fall time | CL=30pF,VDD=2.7-5.5V | | 8 | ns |
| | | | CL=50pF,VDD=2.7-5.5V | | 12 | ns |
| | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | | 10 | | ns |

*Note: Parameters are guaranteed by design.*

### 3.3.11 NRST pin characteristics

Table 3-22 External reset pin characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$[1] | NRST input low voltage | | -0.3 | | 0.8 | V |
| $V_{IH(NRST)}$[1] | NRST input high voltage | | $0.65V_{DD}$ | | $V_{DD}$+0.5 | V |
| $V_{hys(NRST)}$ | Voltage hysteresis of NRST Schmitt trigger | | | 330 | | mV |
| $R_{PU}$[2] | Weak pull-up equivalent resistance | | 30 | 42 | 55 | KΩ |

*Notes: 1. Parameters are guaranteed by design.*

*2. The pull-up resistor is a real resistor connected in series with a switchable PMOS. The resistance of this PMOS/NMOS switch is very small (occupies approximately 10%).*

Reference scheme and requirements:

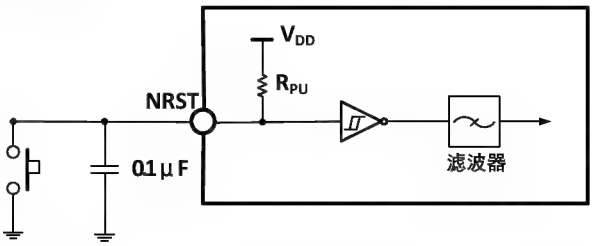


Figure 3-7 Typical application of external reset pin

### 3.3.11 TIM timer characteristics

Table 3-23 TIMx characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | | 1 | | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72MHz | 13.9 | | ns |
| $F_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 72MHz | 0 | 36 | MHz |
| $R_{esTIM}$ | Timer resolution | | | 16 | 位 |
| $t_{COUNTER}$ | 16-bit counter clock period when | | 1 | 65536 | $t_{TIMxCLK}$ |

| | | | | | |
|---|---|---|---|---|---|
| | internal clock is selected | $f_{TIMxCLK}$ = 72MHz | 0.0139 | 910 | us |
| $t_{MAX_COUNT}$ | Maximum possible count | | | 65535 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 72MHz | | 59.6 | s |

*Note: Parameters are guaranteed by design.*

### 3.3.12 I2C interface characteristics

Table 3-24 I2C interface characteristics

| Symbol | Parameter | Standard I2C | | Fast I2C | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.2 | | us |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | us |
| $t_{SU(SDA)}$ | SDA data setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | | 0 | 900 | ns |
| $t_{r(SDA)}/t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | 20 | | ns |
| $t_{F(SDA)}/t_{F(SCL)}$ | SDA and SCL fall time | | 300 | | | ns |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | | 0.6 | | us |
| $t_{SU(STA)}$ | Repeated Start condition setup time | 4.7 | | 0.6 | | us |
| $t_{SU(STO)}$ | Stop condition setup time | 4.0 | | 0.6 | | us |
| $t_{w(STO:STA)}$ | Time from Stop condition to Start condition (bus free) | 4.7 | | 1.2 | | us |
| $C_b$ | Capacitive load for each bus line | | 400 | | 400 | pF |

*Note: Parameters are guaranteed by design.*

### 3.3.12 SPI interface characteristics

Table 3-25 SPI interface characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ | SPI clock frequency | Master mode | | 36 | MHz |
| | | Slave mode | | 36 | MHz |
| $t_{r(SCK)}/t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C=30pF | | 20 | ns |
| $t_{SU(NSS)}$ | NSS setup time | Slave mode | $2t_{PCLK}$ | | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | $2t_{PCLK}$ | | ns |
| $t_{w(SCKH)}/t_{w(SCKL)}$ | SCK high and low time | Master mode, $f_{PCLK}$ = 36MHz, prescaler factor = 4 | 40 | 60 | ns |
| $t_{SU(MI)}$ | Data input setup time | Master mode | 5 | | ns |
| | | Slave mode | 5 | | ns |
| $t_{h(MI)}$ | Data input hold time | Master mode | 5 | | ns |
| | | Slave mode | 4 | | ns |
| $t_{a(SO)}$ | Data output access time | Slave mode, $f_{PCLK}$ = 20MHz | 0 | $1t_{PCLK}$ | ns |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 0 | 10 | ns |
| $t_{V(SO)}$ | Data output valid time | Slave mode (after enable edge) | | 25 | ns |
| $t_{V(MO)}$ | Data output valid time | Master mode (after enable edge) | | 5 | ns |
| $t_{h(SO)}$ | Data output hold time | Slave mode (after enable edge) | 15 | | ns |
| $t_{h(MO)}$ | | Master mode (after enable edge) | 0 | | ns |

### 3.3.13 USB interface characteristics

Table 3-26 USB module characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | USB operating voltage | Disable USB5VSEL control bit | 3.0 | 3.6 | V |
| | | Enable USB5VSEL control bit | 4.0 | 5.5 | |
| $V_{SE}$[1] | Single ended receiver threshold | $V_{DD}$ = 3.3V | 1.3 | 1.9 | V |
| | | $V_{DD}$ = 5V | 1.0 | 1.7 | |
| $V_{OL}$ | Static output low level | | | 0.3 | V |
| $V_{OH}$ | Static output high level | | 2.8 | 3.6 | V |

*Note: 1. Parameters are guaranteed by design.*

### 3.3.14 12-bit ADC characteristics

Table 3-27 ADC characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Supply voltage | | 3.0 | | 5.5 | V |
| $f_{ADC}$ | ADC clock frequency | | | | 14 | MHz |
| $f_S$ | Sampling rate | | | | 1 | MHz |
| $f_{TRIG}$ | External trigger frequency | $f_{ADC}$ = 14MHz | | | 875 | KHz |
| | | | | | 16 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range | | 0 | | $V_{DDA}$ | V |
| $R_{AIN}$ | External input impedance | | | | 58 | KΩ |
| $R_{ADC}$ | Sampling switch resistance | | | 0.6 | 0.75 | KΩ |
| $C_{ADC}$ | Internal sample and hold capacitor | | | 30 | | pF |
| $t_{Iat}$ | Injection trigger conversion latency | $f_{ADC}$ = 14MHz | | | 0.143 | us |
| | | | | | 2 | $1/f_{ADC}$ |
| $t_{Iatr}$ | Regular trigger conversion latency | $f_{ADC}$ = 14MHz | | | 0.143 | us |
| | | | | | 2 | $1/f_{ADC}$ |
| $t_s$ | Sampling time | $f_{ADC}$ = 14MHz | 0.107 | | 17.1 | us |
| | | | 1.5 | | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$ | Power-on time | | | | 1 | us |
| $t_{CONV}$ | Total conversion time (including sampling time) | $f_{ADC}$ = 14MHz | 1 | | 18 | us |
| | | | 14 | | 252 | $1/f_{ADC}$ |

*Note: Parameters are guaranteed by design.*

Formula: $R_{AIN}$ max

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance for an error below 1/4 of LSB. N=12 (from 12-bit resolution).

Table 3-28 $R_{AIN}$ max when $f_{ADC}$ = 14 MHz

| $T_S$ (period) | $t_S$ (us) | $R_{AIN}$ max (KΩ) |
|---|---|---|
| 1.5 | 0.11 | 0 (not recommended) |
| 7.5 | 0.54 | 1.1 |
| 13.5 | 0.96 | 2.6 |
| 28.5 | 2.04 | 6.2 |
| 41.5 | 2.96 | 9.4 |
| 55.5 | 3.96 | 12.9 |
| 71.5 | 5.11 | 16.8 |
| 239.5 | 17.1 | 58 |

*Note: Parameters are guaranteed by design.*

$C_p$ represents the parasitic capacitance (about 5pF) between the PCB and the bonding pad, which may be related to the quality of the bonding pad and PCB layout. A larger $C_p$ value will reduce the conversion accuracy, and the solution is to reduce the $f_{ADC}$ value.

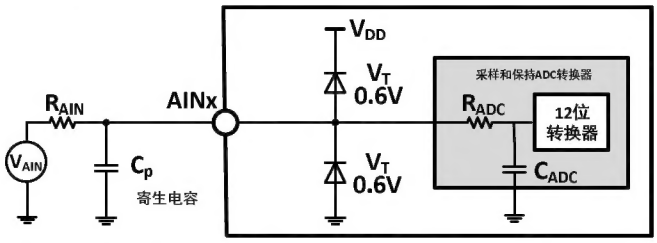


Figure 3-8 Typical connection diagram using the ADC

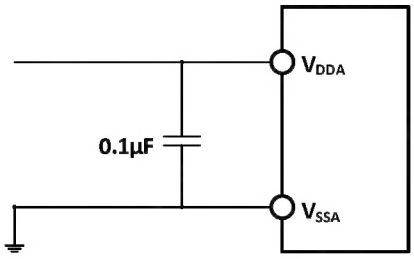


Figure 3-9 Analog power supply and reference decoupling

### 3.3.15 Temperature sensor characteristics

Table 3-29 Temperature sensor characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Avg_Slope | Average slope | | 3.3 | 4.3 | 5.3 | mV/°C |
| $V_{25}$ | Voltage at 25°C | | 1.11 | 1.34 | 1.57 | V |
| $T_{S_temp}$ | ADC sampling time when reading the temperature | $f_{ADC}$ = 14MHz | | | 17.1 | us |

*Note: Parameters are guaranteed by design.*

# Chapter 4 Package information

## Packages

| Package | Body size | Lead pitch | | Description | Part No. |
|---|---|---|---|---|---|
| LQFP48 | 7*7mm | 0.5mm | 19.7mil | Standard LQFP 48-pin patch | CH32F103C6T6 |
| LQFP48 | 7*7mm | 0.5mm | 19.7mil | Standard LQFP 48-pin patch | CH32F103C8T6 |
| QFN48X7 | 7*7mm | 0.5mm | 19.7mil | Quad no-lead 48-pin patch | CH32F103C8U6 |
| LQFP64M | 10*10mm | 0.5mm | 19.7mil | LQFP64M (10*10) patch | CH32F103R8T6 |

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. The error of other dimensions is not more than ±0.4mm or 15%.

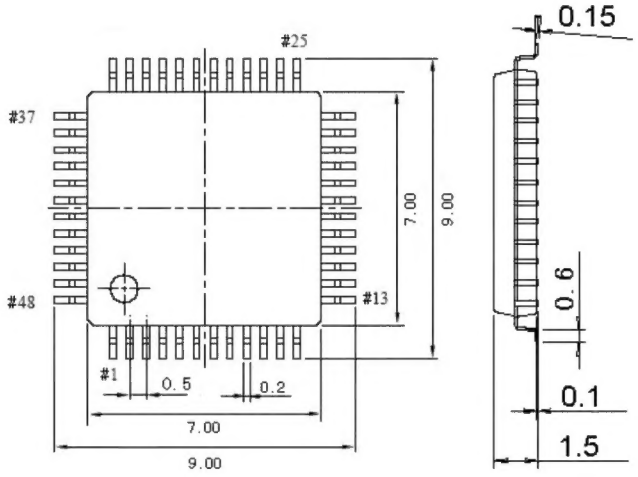


Figure 4-1 LQFP48 outline

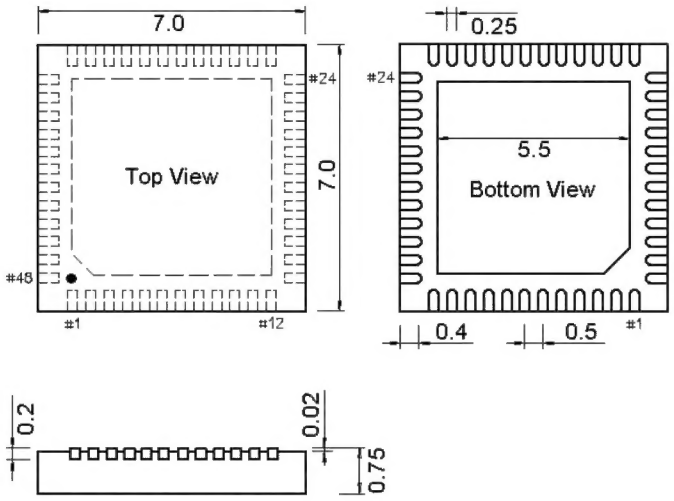


Figure 4-2 QFN48X7 (QFN48-7*7) outline

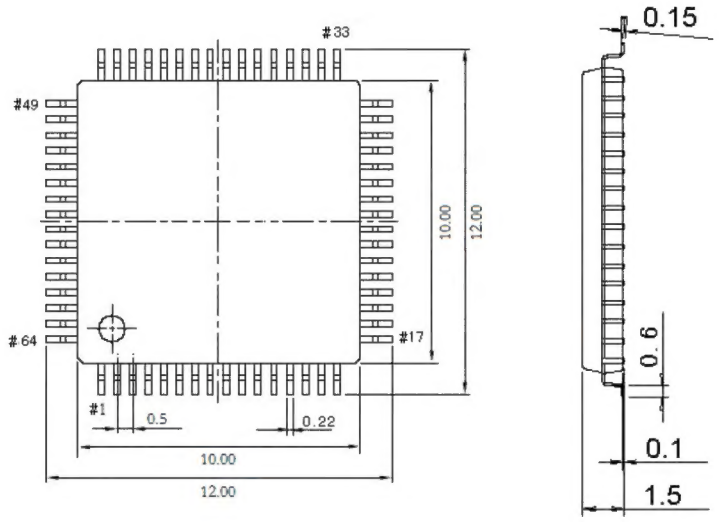


Figure 4-3 LQFP64M (LQFP64-10*10) outline